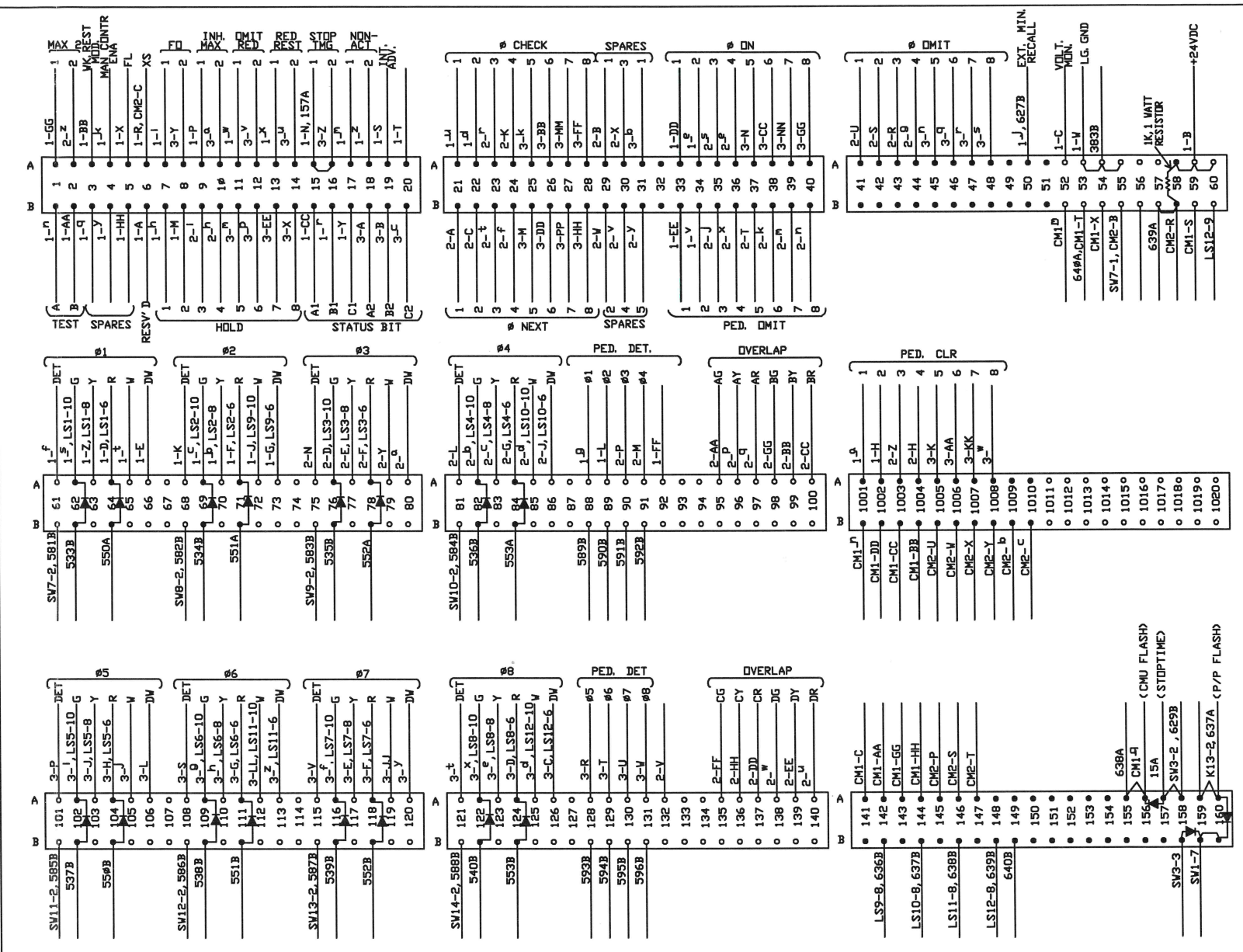
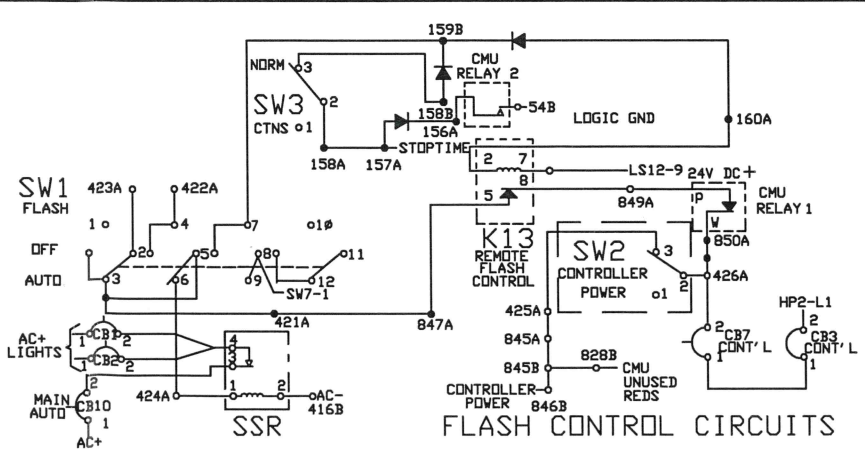
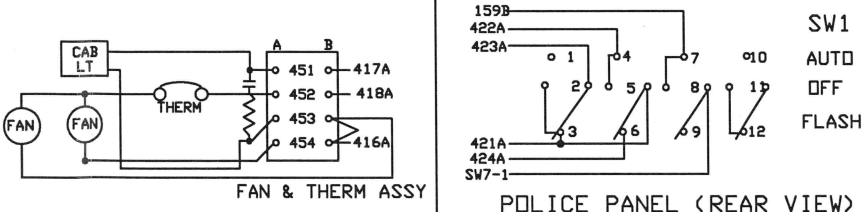
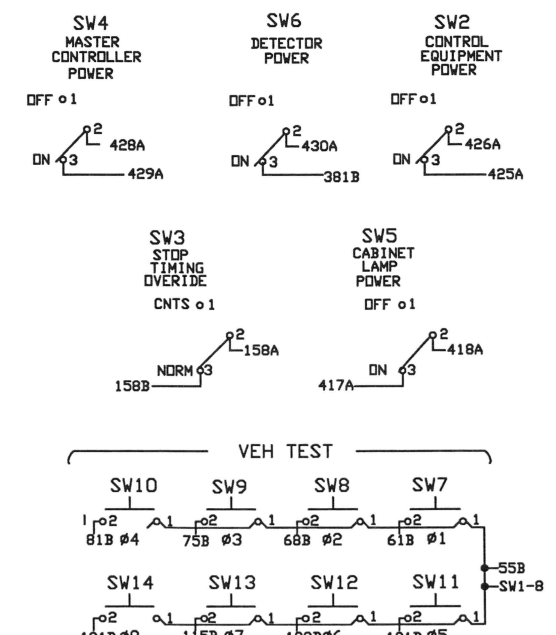


CONTROLLER INTERFACE PANEL

1	2	3
SH SHELL GROUND 1-V	A #1 PHASE NEXT 21B	A STATUS BIT A2 18B
A RESV 6B	B SPARE 1 21A	B STATUS BIT B2 19B
B 24VDC+ 59A	C #2 PHASE NEXT 22B	C #8 DVK 126A
C VOLTAGE MONITOR 52A	D #3 GRN 76A	D #8 RED 124A
D #1 RED 64A	E #3 YEL 77A	E #7 YEL 117A
E #2 RED 66A	F #3 RED 78A	F #6 RED 118A
F #2 RED 71A	G #4 RED 84A	G #5 RED 111A
G #2 DVK 73A	H #4 PCL 1004A	H #5 RED 104A
H #2 PCL 1002A	J #4 DVK 86A	J #5 YEL 103A
J #2 WK 72A	K #4 CHECK 24A	K #5 PCL 1005A
K #2 VEH DET 68A	L #4 VEH DET 81A	L #5 DVK 106A
L #2 PED DET 89A	M #4 PED DET 91A	M #5 PHASE NEXT 25B
M #2 HOLD 8B	N #3 VEH DET 75A	N #5 PHASE DN 37A
N STOP TIMING 1 15A	P #3 PED DET 90A	P #5 VEH DET 101A
P INHIBIT MAX TERM 1 9A	R #3 PHASE DMIT 43A	R #5 PED DET 128A
R EXTERNAL START 6A	S #2 PHASE DMIT 42A	S #6 VEH DET 108A
S INTERVAL ADVANCE 19A	T #5 PED DMIT 37B	T #6 PED DET 129A
T INDICATOR LAMP CONT 20A	U #1 PHASE DMIT 41A	U #7 PED DET 130A
U AC- NEUTRAL NB1	V PED RECYCLE 2 132A	V #8 PED DET 115A
V CHASSIS GROUND GB1	W SPARE 2 29B	W #9 PED DET 131A
W LOGIC GROUND 53A	X SPARE 3 30A	X #8 HOLD 14B
X FLASH LOGIC OUT 5A	Y #3 WK 79A	Y FORCE OFF 2 8A
Y STATUS BIT C1 17B	Z #3 PCL 1003A	Z STDP TIME 2 16A
Z #1 YEL 63A	a #3 DVK 80A	a INHIBIT MAX TERM 2 10A
a #1 PCL 1001A	b #4 GRN 82A	b SPARE 1 31A
b #2 YEL 70A	c #4 YEL 83A	c STATUS BIT C2 20B
c #2 GRN 69A	d #4 WALK 85A	d #8 WK 125A
d #2 CHECK 22A	e #4 PHASE DN 36A	e #8 YEL 123A
e #2 PHASE DN 22A	f #4 PHASE NEXT 24B	f #7 GRN 116A
f #1 VEH DET 34A	g #4 PHASE DMIT 44A	g #6 GRN 109A
f #1 PED DET 61A	h #4 HOLD 10B	h #6 YEL 110A
g #1 HOLD 88A	i #3 HOLD 9B	i #5 GRN 102A
h #1 HOLD 7B	j #3 PED DMIT 35B	j #5 WK 105A
i FORCE OFF 1 7A	k #6 PED DMIT 38B	k #5 CHECK 25A
j EXT MIN RECALL ALL # 50A	m #7 PED DMIT 39B	m #5 HOLD 11B
k MAN. CONTROL ENABLE 4A	n #8 PED DMIT 40B	n #5 PHASE DMIT 45A
l CALL TO NON-ACT I 17A	p #1 A YEL 96A	p #6 HOLD 12B
m TEST INPUT A 1B	q #1 A RED 97A	q #6 PHASE DMIT 46A
n AC+ CONTROL 846B	r #3 CHECK 23A	r #7 PHASE DMIT 47A
o SPARE 1 3B	s #3 PHASE DN 23A	s #8 PHASE DMIT 48A
o STATUS BIT B1 16B	t #3 PHASE NEXT 35A	t #8 VEH DET 121A
s #1 GRN 62A	u #1 D RED 23B	u RED REST MODE 2 14A
t #1 WK 65A	v SPARE 4 30B	v #9 PCL 12A
u #1 CHECK 21A	w #4 PED DMIT 138A	w #9 GRN 1008A
v #2 PED DMIT 34B	x #8 GRN 122A	x #8 DVK 122A
w DMIT RED CLR 11A	y #7 DVK 120A	y #7 WK 120A
x RED REST MODE 1 13A	z #6 DVK 113A	z #6 PCL 113A
y SPARE 2 4B	AA #6 PCL 1006A	AA #6 PCL 1006A
z CALL TO NON-ACT II 18A	BB #1 B YEL 99A	BB #6 CHECK 26A
AA TEST INPUT B 2B	CC #1 A GRN 95A	CC #6 PHASE DN 38A
BB WALK REST MODIFIER 3A	DD #1 C RED 137A	DD #6 PHASE NEXT 26B
CC STATUS BIT A1 15B	EE #1 D YEL 139A	EE #7 HOLD 13B
DD #1 PHASE DN 33A	FF #1 D GRN 135A	FF #8 CHECK 28A
EE #1 PED DMIT 33B	GG #1 B GRN 98A	GG #8 PHASE DN 40A
FF PED RECYCLE 1 92A	HH #1 C YEL 136A	HH #8 PHASE NEXT 28B
GG MAX 2 SELECT 1A		JJ #7 WK 119A
HH SPARE 3 5B		KK #7 PCL 1007A
		LL #6 WK 112A
		MM #7 CHECK 27A
		NN #7 PHASE DN 39A
		PP #7 PHASE NEXT 27B



AUX PANEL (REAR VIEW)



FOLEY AT 121ST

REV. STATUS

REV	DATE	STATUS
1	12/20/02	REVISED

ACT Electronics, Inc.

TITLE: MNDOT 2002 'R' & 'P' CABINET

REV. 1 2 3

SHEET 1 2 3

REV. 1 2 3

